[0014] Having such configuration, larger electrical current can be flowed along the coupling region after the transistor is operated and a snapback is occurred, and then an impact ionization is occurred in a coupling region having an impurity concentration lower than the collector or the drain region or the buried region, thereby providing a function as a second transistor to these regions.

[0015] Here, in order to create the impact ionization in the coupling region after the snapback of the transistor to allow the collector or drain region, the buried region and the coupling region functioning as the second transistor, impurity concentrations in these regions, width of the coupling region along the electric current direction on the path or the like should be suitably controlled.

[0016] According to the present invention, a breakdown voltage can be improved after commencing the operation of the transistor in the semiconductor device including the transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The above and other objects, advantages and features of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

[0018] **FIG. 1** is a cross sectional view of a semiconductor device according to the present invention, illustrating a configuration of a semiconductor device in an embodiment;

[0019] **FIG. 2** is a diagram, showing a profile of an impurity concentration in the cross section broken along an arrow shown in **FIG. 1**;

[0020] **FIGS. 3A and 3B** are cross-sectional views of the semiconductor device according to the present invention, describing an operation of the semiconductor device in the embodiment of the present invention;

[0021] **FIG. 4** is a cross sectional view of a semiconductor device according to the present invention, illustrating an effective base region in the operation of the transistor Q_1;

[0022] **FIGS. 5A, 5B** and **5**C are diagrams, showing conditions of the N-type coupling region in the operation of the transistor Q_1;

[0023] **FIG. 6** is a diagram, showing a profile of a potential difference in the cross section broken along the arrow shown in **FIG. 1**;

[0024] **FIGS. 7A and 7B** are circuit diagrams in the semiconductor device according to the embodiment of the present invention;

[0025] **FIG. 8** is a graph, showing a relationship of the an electrical voltage V_c of the collector with an electrical current I_c flowing through the collector in the semiconductor device of the embodiment according to the present invention;

[0026] **FIGS. 9A, 9B** and **9**C are cross-sectional views of the semiconductor device according to the present invention, illustrating a part of a procedure for manufacturing the semiconductor device in the embodiment of the present invention;

[0027] **FIG. 10** is a schematic plan view of the semiconductor device according to the present invention;

[0028] **FIG. 11** is a cross-sectional view of another exemplary configuration of the semiconductor device shown in **FIG. 1**;

[0029] **FIG. 12A** is a cross-sectional view a configuration of a semiconductor device in the embodiment according to the present invention, and **FIG. 12B** is a schematic plan view thereof;

[0030] **FIG. 13A** is a cross-sectional view a configuration of a semiconductor device in the embodiment according to the present invention, and **FIG. 13B** is a schematic plan view thereof;

[0031] **FIG. 14A** is a cross-sectional view a configuration of a semiconductor device in the embodiment according to the present invention, and **FIG. 14B** is a schematic plan view thereof;

[0032] **FIG. 15A** is a cross-sectional view a configuration of a semiconductor device in the embodiment according to the present invention, and **FIG. 15B** is a schematic plan view thereof;

[0033] **FIG. 16** is a cross-sectional view of an alternative semiconductor device in the embodiment according to the present invention;

[0034] **FIG. 17** is a cross-sectional view of an alternative semiconductor device in the embodiment according to the present invention;

[0035] **FIG. 18** is a cross-sectional view of an alternative semiconductor device in the embodiment according to the present invention;

[0036] **FIG. 19** is a cross-sectional view of a conventional semiconductor device;

[0037] **FIG. 20** is a graph, showing a relationship of an electrical voltage V_c of the collector with an electrical current I_c flowing through the collector in a conventional semiconductor device.

DETAILED DESCRIPTIONS

[0038] The invention will be now described herein with reference to illustrative embodiments. Those skilled in the art will recognize that many alternative embodiments can be accomplished using the teachings of the present invention and that the invention is not limited to the embodiments illustrated for explanatory purposed.

[0039] Preferable embodiments according to the present invention will be described as follows in further detail, in reference to the annexed figures. In all figures, identical numeral is assigned to an element commonly appeared in the figures, and the detailed description thereof will not be presented.

[0040] A semiconductor device according to the present embodiment includes a transistor, through which an electrical current flows via a buried region of the first conductivity type that is the same type of the conductivity as a collector region or a drain region has. In the semiconductor device, a coupling region that is capable of functioning as a second conductivity type region by an impact ionization when the transistor is in an operating state, is disposed on a path including the collector or drain region and the buried region.